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W/ATTACH  
MENT. 6-27-02  
Mush

PATENT

Customer No. 22,852

Attorney Docket No. 04329.2270-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re 53(b) Continuation Application of: )  
)  
Shinsuke SAKAMOTO et al. ) Group Art Unit: 2815  
)  
Application No.: 09/527,563 ) Examiner: E. Lee  
)  
Filed: March 16, 2000 )  
)  
For: SEMICONDUCTOR )  
INTEGRATED CIRCUIT DEVICE )  
AND WIRING ARRANGING )  
METHOD THEREOF )

Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

**PRELIMINARY AMENDMENT**

Prior to the examination of the above application, please amend this application  
as follows:

**IN THE SPECIFICATION:**

Please amend the specification as follows:

On page 1, replace the paragraph beginning on line 11 with the following:

A1 The present invention relates to a semiconductor integrated circuit device making  
use of an area pad and a wiring arranging method thereof.

On page 9, replace the paragraph beginning on line 22 with the following:

A2 As described above, the wiring length of the I/O slot can be shortened by the  
rewiring 24, 33 on the outermost periphery of the chip, and the delay in the signal

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